METEORCOMM LLC

Test Strategy Development

For the Locomotive Radio, Base Radio, and Wayside Radio Products

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Revision History

Revision	Date	Summary of Changes
1.0	12/19/2012	First draft FRA document.

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Rev 2.0

Introduction

This document has been prepared to define a recommended test strategy for the subject products. This document will include the following sections:

- Test Strategy Matrix
- General Test Descriptions
- Specific Test Descriptions
    - Pre-Production
    - Capacity Estimates
- Information Architecture

The scope of this strategy is limited to pre-production. As the products enter production phase, the test strategy will be refined to optimize for efficentcy and cost.

Definitions

PA: Power Amplifier
LED: Light Emmiting Diode
RF: Radio Frequency
IDQ: Quiescent current
DC: Direct Current
T/R: Transmit Receive
LPF: Low Pass Filter
AOI: Automatic Optical Inspection
AXI: Automatic X-ray inspection (generally 2 dimensional)
FP: Flying probe
PCB: Printed circuit board (bare, unpopulated)
ICT: In circuit test
DPMO: Defects per Million Opprotunity
OCR: Optical Character Recognition
FCT: Functional Test
IC: Integrated Circuit
Gage R&R: Gage, Repeatability and Reproducibility
BGA: Ball Grid Array
CPLD: Complex Programable Logic Device
LVDS: Low Voltage Differential Signaling
RX: Recieve
BER: Bit Error Rate
LO: Local Oscillator
IQ : Orthoganal modulating signals (I-Q) in a quadrature amplitude modulation system
GPS: Global positioning system
SD: Secure Digital
ADC: Analog Digital Converter
PCBA: Printed Circuit Board Assembly (populated board)
XO: Crystal Oscillator
USB: Universal Serial Bus
SPI: Serial Peripheral Interface
I^2C: Inter-Integrated Circuit;
DQPSK: Differential Quadrature Phase Shift Keying
POST: Power On Self Test
LAN: Local Area Network

Test Strategy Matrix Summary

		Pre-Production Test				
		No Test	AOI	AXI	Flying Probe	Functional Test
Locomotive Radio						
	Master Board		X	X	X	1
	Power Supply Board		X		X	2
	PA/Modulator Board		X		X	
	Front End Board		X		X	
	LED Board		X			
	PA/Modulator IDQ Current Tune (RF Module Subassembly)					3
	PA/Modulator Tune (Final Assembly)					4
	Final Assembly					5
Base Radio						
	Master Board		X	X	X	1
	Power Supply Board		X		X	2
	PA/Modulator Board		X		X	
	Front End Board		X		X	
	LED Board		X			
	Ethernet Board		X			
	PA/Modulator IDQ Current Tune (RF Module Subassembly)					3
	PA/Modulator Tune (Final Assy)					4
	Final Assembly					5
Wayside Radio						
	Master Board		X	X	X	6
	RF/DC Power Distribution Board		X		X	
	T/R Switch, Coupler, and Low Pass Filter Board		X		X	
	Sub-Assy (RF/DC Power, LPF, Chassis)	X				
	Final Assy					7

General Test Descriptions

The information in this section defines in general terms each of the inspection and test strategies reviewed for this product. Typically, AOI, AXI, and FP are production inspection strategies that are developed by the PCB manufacturer based on factory equipment. ICT is a test solution that can be developed by third party developers for manufacturing as long as ICT tester configuration information is available to the ICT developer. Functional test can be developed and transitioned into the board manufacturer when complete.

General Data Reporting Requirements

First pass yield and Pareto will be calculated and maintained at each test process. A DPMO goal of 450 has been established for the PCBA level testing. Corrective investigation and action will be performed on any assembly that exceeds this DPMO goal.
All test failures will be directed to a troubleshooting center for failure analysis. This trouble shooting center may reside in-line, depending on the level of assembly and manufacturing strategy for that level. Rework shall be performed by trained personelle, according to IPC standards. Repair will not be done without prior authorization.

Automated Optical Inspection (AOI)

With Automated Optical Inspection (AOI), a series of digital pictures of the areas of interest on the PCB Assembly are taken. Then, machine application software compares specific images within the pictures to templates of known good images created from known good boards based on human inspection according to IPC 610 E. When differences occur that drop a correlation score below a programmed threshold, the software flags missing components, misaligned components, wrong (size) components and polarity (if polarity markings or features exist). The system may also do a level of OCR (Optical character recognition) to perform part number verification when text quality and repeatability are acceptable. AOI can detect a level of visible solder shorts and opens, but hidden or marginal solder joints would not be identified. AOI will be performed on 100% of machine placed components

Automated X-ray Inspection (AXI)

Automated X-ray Inspection (AXI), as the name is implies, is not a test but an inspection aid used to locate structural solder defects early in the process, before they impact more costly downstream test and assembly operations. X-ray is only applied at the board level. Through automatic X-ray image acquisition and analysis, virtually all of the solder joints on an assembly can be verified as defect free in a mater of minutes. This includes the joints that are hidden from visual inspection, such as grid-array packages and some connector styles. The algorithms used during image analysis not only allow for detection of ‘hard fails’, such as open joints and solder bridges, but also potential latent issues such as insufficient solder, excessive solder, and voiding which may be missed by all other test and inspection methods. Polarity of most tantalum SMT capacitors is also detectable. Due to the relatively low programming time and cost, AXI is an excellent tool for verifying proto-type assemblies. AXI is often used as part of a combinational strategy with Flying Probe (Fixtureless) Test during proto-type and pilot phases, and then kept in place once ICT and/or Function Test is implemented as part of an overall test and inspection strategy.

Flying Probe Test (FP)

Flying Probe Test is generally used for the detection of manufacturing process defects at the board level. Typical defects found are wrong component populated, missing component, wrong orientation of the component, and solder bridges. A number of factors determine if these failure modes can be detected. Due to board probe-ability, topology, circuit configuration, or part type, these failure modes may not be detectable for all components. 100% test coverage is not attainable at Flying Probe due to the non-powered test method. Component functionality can not be verified on such component types as voltage regulators and IC’s. By-pass caps, connectors, and tantalum cap polarities are also not typically testable at Flying Probe, although shorts may still be detected. While Flying Probe is more flexible with regards to test access than a typical ICT test, board design should still try to maximize test coverage for ICT and Flying Probe. Flying Probe development time is relatively fast, and development cost is relatively inexpensive, making it an excellent solution for proto-types and as an interim test prior to ICT implementation. However, the test time is significantly longer than a typical ICT test so it does not lend itself well to on-going production except in extremely low volume applications. Often the Flying Probe is used in a combinational strategy with Automated X-ray Inspection until an ICT strategy can be implemented.

Functional Test (FCT)

Functional test can be applied with varying degrees of comprehensiveness. , the need for a very comprehensive functional test is paramount. Functional test in this case is applied to test component presence, orientation, connectivity and functionality. If a strong ICT test solution is in place the functional test is reduced to testing functionality. The level of test in this case is often reduced to testing critical board functions or known troublesome circuits. Fortuitously, if a functional test is applied it is sometimes easy to add additional functional test with little effort using the same instruments as required for the critical function testing. Functional test configurations can be pseudo hot-mock-up testing by exercising the circuits with mating products mimicking test at the final product level. Though the implementation varies, functional tests are applied at the board and system level during product manufacturing.Test procedures and limilts are controlled via separate Test Requirements Specifications.
Often the Functional Test solution is used to exercise critical functionality test and system acceptance tests. These test requirements are typically specified in the system test requirements specification. The configuration and documentation control levels are typically high when a test solution contains acceptance testing.

Stress test audits

Stress testing of some form is called for by contract as burn-in over operating temperature range. The Reliability and Test community of both CalAmp and MCC agree that this requirement is insufficiently defined and that a traditional 100% burn-in is ineffective. A separate, burn-in alternative process is currently being discussed and will be defined in a separate document.

Specific Test Descriptions

The numbered items in the test matrix will each have a description in this section that defines the tests to be performed.

Pre-Production Testing

Pre-production functional testing will consist of semi-automated or computer guided testing similar to what was with field and reliability production, with additional automation. All automation is accomplished via TestStand and LabVIEW for instrumentation control, measurement and analysis. TestStand and LabVIEW would provide test report capability for storing test history and simple integration with most manufacturing execution systems.
Pre-production test systems will be validated by means of Gage R&R studies. The studies have been conducted as part of the field and reliabitliy build and will be repeated using the pre-production test system when samples are available. Gage R&R studies should be performed on all production test systems.
All tests will be performed on calibrated, NIST traceable systems. A library of known good and known bad units will be created for pre-production. These units will be used to validate the test system at prescribed intervals.

1 - Master Board Test (Locomotive Radio and Base Radio)

The pre-production test strategy for testing the Locomotive Radio and Base Radio Master board will consist of AXI testing for early detection of BGA and leadless package solder defects. Flying Probe test will be utilized for electrical test of continuity/shorts testing and basic component placement detection. AOI will be performed, providing defect detection coverage for the entire assembly. Human visual inspection will be performed according to IPC A610 Rev. E class II. BGA components are inspected via

AXI. In addition to this standard, defect "hot spots" identified during the field and reliability builds will receive special attention by inspection at increased magnification.
Master board functional testing will be used to provide fault coverage for;

- Verify power to ground continuity – check for shorts
- Verify current draw
- Verify power rails
- Verify and/or Program the CPLD
- Verify and/or Program the Coldfire Bootloader
- Verify power-up/reset circuitry
- Verify power enable circuit
- Power On Self Test
- Temperature Sensor Test
- Verify clocks
- Verify LVDS clocks
- Verify Serial Port
- Verify Ethernet Circuitry – LAN and Maintenance Ports
- Verify LED circuitry using known good LED board
- Verify Fans using known good fans and/or DC Electronic Load (Base Radio only)
- Verify RX circuitry (Bit Error Rate – BER testing)
- Verify 440MHz Linear PA LO
- Verify IQ Modulator outputs (TXQ+_980, TXQ-_980, TXI+_980, and TXI-_980)
- Verify GPS circuitry (Base Radio only)
- Verify SD card port

Testing listed above will require operator interaction for connecting instrumentation and for connecting required interface connections. Communication to the instrumentation and data analysis would be automated via TestStand and LabVIEW.

2 – Power Supply Board Test (Locomotive Radio and Base Radio)

The pre-production test strategy for testing the Locomotive Radio and Base Radio Power Supply board will consist of AOI testing for early detection of gross defects, Flying Probe test for electrical continuity/shorts testing and basic component placement detection. Human visual inspection will be performed according to IPC A610 Rev. E class II. In addition to this standard, a particular component (voltage regulator) will be audited via AXI as it was identified as problematic in the field radio builds.

Power Supply board functional testing, without a power brick installed, will consist of the following:

- Verify continuity on power to ground – check for shorts
- Verify continuity between power supply input and brick input
- Verify +12V power rail w/ applied nominal V at power brick output
- Verify +12V voltage regulation with applied current load
- Verify converter outputs on J3

Power Supply board functional testing, with a power brick installed, will consist of the following:

- Verify continuity on power to ground – check for shorts
- Verify power rails
- Verify current draw
- Verify voltage regulation with applied current load
- Verify converter outputs on J3

Testing listed above will require operator interaction for connecting instrumentation and for connecting required interface connections. Communication to the instrumentation and data analysis will be automated via TestStand and LabVIEW.

3 – PA/Modulator IDQ Current Tune – RF Module Subassembly (Locomotive Radio and Base Radio)

The pre-production test strategy for testing the Locomotive Radio and Base Radio RF Module subassembly will consist of tuning the Idq currents on the PA/Modulator board within the RF Module subassembly.

For the Base Radio the RF Module assembly at this step will consist of the PA/Mod PCBA, Front End PCA, and circulator mounted to the RF baseplate and heat sink.

For the Locomotive Radio the RF Module assembly at this step will consist of the PA/Mod PCBA, Front End PCBA, and Power Supply PCBA mounted to the final assembly chassis.

The tuning procedure involves tuning VR2 potentiometer (for driver amplifier) and VR1 potentiometer (for final amplifier) while monitoring the voltage at R8 and R5 respectively. The approach for pre-production will be to monitor these voltages, via software, using a USB SPI/I^2C device which communicates with the ADC on the PA/Mod PCBA. The ADC circuitry is connected to R8 and R5 on the PA/Mod PCBA. The software would show the operator where the measurement lies allowing tuning of the potentiometers to the desired value within the accepted range. Upon reaching an acceptable value the potentiometers will be glued to prevent further adjustment.

TestStand/LabVIEW would be utilized to control the USB SPI/I^2C device, provide instruction to the operator, and to record the tuning results in an appropriate report.

4 – PA/Modulator Tune – Final Assembly (Locomotive Radio and Base Radio)

The pre-production test strategy for tuning the Locomotive Radio and Base Radio final assembly will consist of performing an open loop PA check and a closed loop PA check, tuning I/Q DC offset parameters (LO leakage), tuning CML phase, tuning Igain and Qgain parameters (power output), and tuning XO setting (reference clock). All testing/calibration performed at this level will be performed within a shielded RF enclosure, if necessary (RF isolation may be avoided via spectrum management and spatial diversity). TestStand/LabVIEW would be utilized to control all instrumentation, provide instruction to the operator for cable connections, etc., to perform all communication to the device under test for device settings/calibration values, and to record the tuning results in an appropriate report.

For both the Base Radio and Locomotive Radio the subassembly at this step will consist of the entire final assembly.

An open loop PA check and closed loop PA check would be performed to include a quick power on/current draw test and to measure the RF output power with DQPSK modulation transmission.

The LO leakage tuning would involve tuning the IDC and QDC baseband tuning parameters until the desired LO leakage is achieved. The calibration value would be stored in the Master board
The CML phase tuning would involve adjusting the CML phase until the desired result is achieved. The calibration value would be stored in the Master board.

The power output tuning would involve adjusting the I and Q gain values until the desired power output is achieved. The calibration value would be stored in the Master board.

The reference clock tuning would involve adjusting the XO setting until the desired relative frequency error is achieved. The calibration value would be stored in the Master board and retained in the relevant manufacturing database, need this in database section or every paragraph.

5 - Final Test (Locomotive Radio and Base Radio)

The pre-production test strategy for final device level test will include the testing listed below. All testing performed at this level will be performed on a fully assembled unit within a shielded RF enclosure, if necessary (RF isolation may be avoided via spectrum management and spatial diversity). TestStand/LabVIEW would be utilized to control all instrumentation, provide instruction to the operator for cable connections, etc., to perform all communication to the device under test, and to record the testing results in an appropriate report.

- Verify current draw under power on, RX, TX, and power save conditions
- Power On Self Test (POST)
- Verify LEDs On/Off
- Verify Fan functionality (Base Radio only)
- Verify Temperature Sensors
- Verify Serial Port
- Verify Ethernet Circuitry – LAN and Maintenance Ports
- GPS Receive Test (Base Radio only)
- TX/RX Receive Bit Error Rate testing at Low/Mid/High Frequency,Low/Mid/High supply voltage at π/4 DQPSK
- Primary RX Receive Bit Error Rate testing at Low/Mid/High Frequency, Low/Mid/High supply voltage and π/4 DQPSK (Base Radio Only)
- Diversity RX Receive Bit Error Rate testing at Low/Mid/High Frequency and Low/Mid/High supply voltage and π/4 DQPSK
- Transmit Output Power at Low/Mid/High Frequency and Low/Mid/High supply voltage for π/4 DQPSK
- Transmit Frequency Accuracy at Low/Mid/High Frequency, Low/Mid/High supply voltage and π/4 DQPSK
- Transmit Modulation Error at Low/Mid/High Frequency, Low/Mid/High supply voltage for π/4 DQPSK
- Transmit Sideband Spectrum at Mid Frequency Mid supply voltage at π/4 DQPSK
- Adjacent Channel Power Ratio at π/4 DQPSK modulation
- Verify SD card interface

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6 - Master Board Test (Wayside Radio)

The pre-production test strategy for testing the Wayside board will consist of AXI testing for early detection of BGA and leadless package solder defects. Flying Probe test will be utilized for electrical test of continuity/shorts testing and basic component placement detection. AOI will be performed, providing defect detection coverage for the entire assembly. Human visual inspection will be performed according to IPC A610 Rev. E class II. In addition to this standard, defect "hot spots" identified during the field and reliability builds will receive special attention by inspection at increased magnification.

Master board functional testing would be used to:

- Verify power to ground continuity – check for shorts
- Verify current draw
- Verify power rails
- Verify and/or Program the CPLD
- Verify and/or Program the Coldfire Bootloader
- Verify power-up/reset circuitry
- Verify power enable circuit
- Power On Self Test
- Temperature Sensor Test
- Verify clocks
- Verify LVDS clocks
- Verify Ethernet Circuitry
- Verify LED circuitry
- Verify RX circuitry (Bit Error Rate – BER testing)
- Verify TX circuitry – CW signal measurement
- Verify GPS circuitry
- TCXO tune and TX check (gross check performed with oscilloscope – final check with spectrum analyzer to be performed at device level test)
- Verify SD card port

Testing listed above will require operator interaction for connecting instrumentation and for connecting required interface connections. Communication to the instrumentation and data analysis will be automated via TestStand and LabVIEW.

7 - Final Test (Wayside Radio)

The pre-production test strategy for final device level test will include the testing listed below. All testing performed at this level will be performed on a fully assembled unit within a shielded RF enclosure, if necessary (RF isolation may be avoided via spectrum management and spatial diversity). TestStand/LabVIEW would be utilized to control all instrumentation, provide instruction to the operator for cable connections, etc., to perform all communication to the device under test, and to record the testing results in an appropriate report.

- Verify current draw under power on, RX, TX, and power save conditions
- Power On Self Test (POST)
- Verify LEDs On/Off
- Verify Temperature Sensors
- Verify Ethernet Circuitry – LAN and Maintenance Ports
- GPS Receive Test
- RX Bit Error Rate testing at Low/Mid/High Frequency and Low/Mid/High supply voltage and π/4 DQPSK

- Transmit Output Power at Low/Mid/High Frequency and Low/Mid/High supply voltage and π/4 DQPSK
- Transmit Frequency Accuracy at Low/Mid/High Frequency and Low/Mid/High supply voltage and π/4 DQPSK
- Transmit Modulation Error at Low/Mid/High Frequency and Low/Mid/High supply voltage and π/4 DQPSK
- Transmit Sideband Spectrum at Mid Frequency Mid supply voltage at π/4 DQPSK
- Adjacent Channel Power Ratio and π/4 DQPSK
- TCXO tune and TX check
  Note: The above wayside transmit test are done at 8 Kps.

Capacity Estimates

The estimated test time for all board level tests combined is 15 minutes. For all unit level testing the expected test time is 30 minutes. A single board level test fixture will be able to deliver a 32 fully test boards per 8 hour shift, assuming line management of this resource will allow it to run continuously thru breaks. The unit level test will deliver a fully tested unit at a rate of 16 per shift with the same line management assumption.

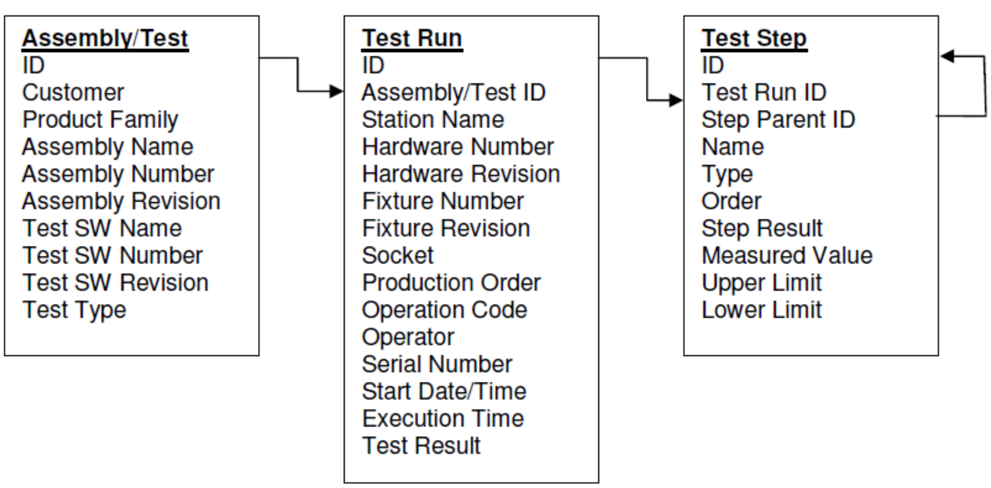
Information Architecture

Test Data Collection Overview

The information associated with and/or generated by a run of a test program is to be managed by systems and architectures which are specific to a given manufacturer. A relevant test related common data model standard is not known. Development of such a model is an appropriate task for industry organizations such as the American Association of Railroads. For the purposes of pre-production CalAmp is creating a rudimentary database tailored to CalAmp's manufacturing systems. Reports can be made available as requested in conventional formats.
Generically, this data is separated into three main categories:

1. Assembly/Test: Information related to assembly that was tested and the test program that tested it.
2. Test Run: Information that is (or can be) unique to a specific run of the test program.
3. Test Step: Information unique to a specific test step that was executed during the run of the test.

Each Assembly Test entity can have one or more Test Run entities associated with it.
Each Test Run entity can have one or more Test Step entities associated with it.
A Test Step entity can have one or more other Test Step entities associated with it (allowing for a hierarchical structure)



This information can be progressively filtered by any of the pieces of information in any of the categories. This allows the reports to be as specific (or general) as they need be.
There are four types of Test Steps

- Parent: A test step that acts as a “container” for other test steps. This allows the test steps to have a hierarchical structure.
- Pass/Fail: A test step that either passes or fails (i.e. a Go/No-Go test).
- Numeric: A test step that gathers and/or measures numeric values.
- String: A test step that gathers and/or measures string values.

A variety of reports can be generated from the test data to include (but not limited to):

- Test Result reports that display the measured values and/or results of the test steps in a test run.
- Statistical analysis on numeric data (Cp, Cpk, StdDev, Mean, etc…)
- Histograms of test step measurements
- Run time charts of test step measurements
- Failure Pareto graphs
- Tester Utilization
- First Pass Yield